

Amendments to the Specification:

Please replace paragraph [0008] with the following amended paragraph:

- 5 [0008] As shown in Fig.2, a thermal growth process is performed to oxidize the exposed epitaxial layer 16 to an oxide layer 24, which fills in the opening 22, with a top surface of the oxide layer 24 being approximately equal to a top surface of silicon dioxide layer 18. After that, the remained ~~silicon nitride layer 24~~ silicon nitride layer 20 is removed. During thermal growth of the oxide layer 24, the dopants of the N⁺ region 12 and the P⁺ region 14 are diffused further upward to broaden the N⁺ region 12 and P⁺ region 14. Afterwards, a photoresist layer 26 is deposited on the oxide layer 24, and the photoresist layer 26 is exposed and developed to form an opening 27 in the photoresist layer 26. Then, suitable N-type dopants, such as phosphorus (P), are ion implanted through the opening 27 to form an N⁺ collector region 28 within the 10 epitaxial layer 16 and beneath the oxide layer 24.
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Please replace paragraph [00025] with the following amended paragraph:

- 20 [0025] As shown in Fig.8, a thermal growth process or a CVD process is performed to form a silicon dioxide layer 92, which has a thickness of about 1300 Å, on the dielectric layer 84. Then, a ~~silicon nitride layer 74~~ silicon nitride layer 94 and an in-situ doped P-type polysilicon layer 96 are formed on the silicon dioxide layer 92, respectively. Further, a patterned photoresist layer (not shown in Fig.8) is formed on 25 the polysilicon layer 96, and a photolithographic and etching process is performed to form an opening 98 in the polysilicon layer 96, the silicon nitride layer 94, the silicon oxide layer 92, and the dielectric layer 84, and a portion of the epitaxial layer 74 is exposed. The in-situ doped P-type polysilicon layer 96 is used as an extrinsic base of the BJT for controlling the electrode voltage of the BJT.

30 *OK to later.*

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